	L #	Hits	Search Text	DBs	Time Stamp
1	L2	622647	(flip adj chip or BGA or (ball adj grid) or IC or device or package or die or dice or dies) near8 (board or substrate or wafer or PCB or (print adj circuit adj board) or MCM or multi-chip or (multi adj chip) or interposer or leadframe or (lead adj frame))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
2	L3	3313687	(diisocyanate adj monomers) or (diisocynate adj end-capped adj compliant adj olgomer) or (ptoluenesulfonyl adj semicarbazide) or (hydroxyl adj end-capped adj oligomer) or (carboxylic adj acid adj polymer) or water or "H.sub.2O" or (polymer$6 near2 foam$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
3	L4	60741	((diisocyanate adj monomers) or (diisocynate adj end-capped adj compliant adj olgomer) or (ptoluenesulfonyl adj semicarbazide) or (hydroxyl adj end-capped adj oligomer) or (carboxylic adj acid adj polymer) or water or "H.sub.2O" or (polymer$6 near2 foam$6)) near4 (filling or filler or infill or insulat$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24

	L #	Hits	Search Text	DBs	Time Stamp
4	L5	1840	(((diisocyanate adj monomers) or (diisocynate adj end-capped adj compliant adj olgomer) or (ptoluenesulfonyl adj semicarbazide) or (hydroxyl adj end-capped adj oligomer) or (carboxylic adj acid adj polymer) or water or "H.sub.2O" or (polymer$6 near2 foam$6)) near4 (filling or filler or infill or insulat$4)) and ((flip adj chip or BGA or (ball adj grid) or IC or device or package or die or dice or dies) near8 (board or substrate or wafer or PCB or (print adj circuit adj board) or MCM or multi-chip or (multi adj chip) or interposer or leadframe or (lead adj frame)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
5	L6	3310554	(diisocyanate adj monomers) or (diisocynate adj end-capped adj compliant adj olgomer) or (ptoluenesulfonyl adj semicarbazide) or (hydroxyl adj end-capped adj oligomer) or (carboxylic adj acid adj polymer) or water or (polymer$6 near2 foam$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24

	L #	Hits	Search Text	DBs	Time Stamp
6	L7	113279	((diisocyanate adj monomers) or (diisocynate adj end-capped adj compliant adj olgomer) or (ptoluenesulfonyl adj semicarbazide) or (hydroxyl adj end-capped adj oligomer) or (carboxylic adj acid adj polymer) or water or (polymer$6 near2 foam$6)) near4 (filling or filler or infill or insulat$4 or support$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
7	L8	829700	interconnect$6 or inter-connect$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
8	L9	2515359	reaction or react$6 or polymerization	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
9	L10	2152580	substrate or wafer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24

	L #	Hits	Search Text	DBs	Time Stamp
10	L11	29699	polymer$4 near2 (foam$6 or bubbles or spray$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
11	L12	53452	(expose$4 or top or surface) near4 (interconnect$6 or inter-connect$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
12	L13	23417	polymer$4 near2 foam$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
13	L14	537	(polymer$4 near2 foam$6) near4 (substrates or wafers)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24

	L #	Hits	Search Text	DBs	Time Stamp
14	L15	605	(polymer$4 near2 foam$6) same interconnect$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
15	L16	544	(438/782).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
16	L17	2503	((438/762).CCLS.) or ((438/765).CCLS.) or ((438/780).CCLS.) or ((438/782).CCLS.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
17	L18	1611	(438/780).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24

	L #	Hits	Search Text	DBs	Time Stamp
18	L34	37708	substrates near8 interconnect$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
19	L35	26656	(second! adj (substrate or wafer)) same (first adj (substrate or wafer))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
20	L36	1001	((second! adj (substrate or wafer)) same (first adj (substrate or wafer))) same interconnect$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
21	L37	929	(((second! adj (substrate or wafer)) same (first adj (substrate or wafer))) same interconnect$6) and ((@ad<"20030620") or (@rlad<"20030620"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24

	L #	Hits	Search Text	DBs	Time Stamp
22	L21	6	(((expose$4 or top or surface) near4 (interconnect$6 or inter-connect$6)) same (reaction or react$6 or polymerization) same (substrate or wafer)) and (polymer$4 near2 (foam$6 or bubbles or spray$6))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
23	L25	20	((polymer$4 near2 foam$6) near4 (substrates or wafers)) same interconnect$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
24	L26	24	((polymer$4 near2 foam$6) near4 (substrates or wafers)) same (inject$6 or spray$6 or diffus$6 or immers$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
25	L28	9	(((438/762).CCLS.) or ((438/765).CCLS.) or ((438/780).CCLS.) or ((438/782).CCLS.)) and (polymer$4 near2 foam$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24

	L #	Hits	Search Text	DBs	Time Stamp
26	L32	77	(((polymer$4 near2 foam$6) near4 (substrates or wafers)) and interconnect$6) and ((@ad<"20030620") or (@rlad<"20030620"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
27	L1	175	(((diisocyanate adj monomers) or (diisocynate adj end-capped adj compliant adj olgomer) or (ptoluenesulfonyl adj semicarbazide) or (hydroxyl adj end-capped adj oligomer) or (carboxylic adj acid adj polymer) or water or "H.sub.2O" or (polymer$6 near2 foam$6)) near4 (filling or filler or infill or insulat$4)) same ((flip adj chip or BGA or (ball adj grid) or IC or device or package or die or dice or dies) near8 (board or substrate or wafer or PCB or (print adj circuit adj board) or MCM or multi-chip or (multi adj chip) or interposer or leadframe or (lead adj frame)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24

	L #	Hits	Search Text	DBs	Time Stamp
28	L19	175	(((diisocyanate adj monomers) or (diisocynate adj end-capped adj compliant adj olgomer) or (ptoluenesulfonyl adj semicarbazide) or (hydroxyl adj end-capped adj oligomer) or (carboxylic adj acid adj polymer) or water or "H.sub.2O" or (polymer$6 near2 foam$6)) near4 (filling or filler or infill or insulat$4)) same ((flip adj chip or BGA or (ball adj grid) or IC or device or package or die or dice or dies) near8 (board or substrate or wafer or PCB or (print adj circuit adj board) or MCM or multi-chip or (multi adj chip) or interposer or leadframe or (lead adj frame)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
29	L30	171	(438/765).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
30	L27	255	((polymer$4 near2 foam$6) same interconnect$6) and (substrate or wafer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24

	L #	Hits	Search Text	DBs	Time Stamp
31	L33	249	(((polymer$4 near2 foam$6) same interconnect$6) and (substrate or wafer)) and ((@ad<"20030620") or (@rlad<"20030620"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
32	L20	320	(((diisocyanate adj monomers) or (diisocynate adj end-capped adj compliant adj olgomer) or (ptoluenesulfonyl adj semicarbazide) or (hydroxyl adj end-capped adj oligomer) or (carboxylic adj acid adj polymer) or water or (polymer$6 near2 foam$6)) near4 (filling or filler or infill or insulat$4 or support$4)) same ((flip adj chip or BGA or (ball adj grid) or IC or device or package or die or dice or dies) near8 (board or substrate or wafer or PCB or (print adj circuit adj board) or MCM or multi-chip or (multi adj chip) or interposer or leadframe or (lead adj frame)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24

	L #	Hits	Search Text	DBs	Time Stamp
33	L23	367	(((expose$4 or top or surface) near4 (interconnect$6 or inter-connect$6)) same (reaction or react$6 or polymerization) same (substrate or wafer)) and ((flip adj chip or BGA or (ball adj grid) or IC or device or package or die or dice or dies) near8 (board or substrate or wafer or PCB or (print adj circuit adj board) or MCM or multi-chip or (multi adj chip) or interposer or leadframe or (lead adj frame)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
34	L24	334	(polymer$4 near2 (foam$6 or bubbles or spray$6)) and ((expose$4 or top or surface) near4 (interconnect$6 or inter-connect$6))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
35	L29	391	(438/762).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24

	L #	Hits	Search Text	DBs	Time Stamp
36	L38	337	((((second! adj (substrate or wafer)) same (first adj (substrate or wafer))) same interconnect$6) and ((@ad<"20030620") or (@rlad<"20030620"))) and polymer$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
37	L22	584	((expose$4 or top or surface) near4 (interconnect$6 or inter-connect$6)) same (reaction or react$6 or polymerization) same (substrate or wafer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:24
38	L31	80	((polymer$4 near2 foam$6) near4 (substrates or wafers)) and interconnect$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:46
39	L39	588	(257/618).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:46

	L #	Hits	Search Text	DBs	Time Stamp
40	L41	1699	((438/107) or (438/109)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:47
41	L42	459	39 and ((@ad<"20030620") or (@rlad<"20030630"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:49
42	L44	130	42 and interconnect$6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:49

	L #	Hits	Search Text	DBs	Time Stamp
43	L45	23	44 and (second near (substrate or wafer))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 16:50
44	L46	604	(257/620).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/08 17:31

DOCUMENT-IDENTIFIER: **US 20030203663 A1**

TITLE: Electrical interconnect using locally conductive adhesive

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Pre-Grant Publication Document Identifier - DID (1):
US 20030203668 A1

Summary of Invention Paragraph - BSTX (15):
[0013] In yet another preferred embodiment, the invention is an electrical **interconnect comprising: (a) a first substrate having a surface** and at least one first electrical contact projecting from the first **substrate** surface; (b) a second **substrate** having a surface and at least one second electrical contact projecting from the second **substrate** surface and aligned with the first electrical contact, such that the first **substrate** surface is substantially parallel to the second **substrate** surface; and, (c) an adhesive interposed between and in contact with the first electrical contact and the second electrical contact, the adhesive comprising an electrically non-conductive resin and particles, the particles comprising a core of at least one electrically conductive **reactive** material and a breakable coating of at least one electrically non-conductive material, the core comprising: (1) at least one first subparticle comprising a **reactive** resin, having conductive material therein, encapsulated inside a rupturable membrane; and, (2) at least one second subparticle comprising a catalyst encapsulated inside a rupturable membrane, wherein the first electrical contact is positioned close enough to the second electrical contact to break the breakable coating of the particles in the interposed adhesive such that the first subparticle membrane and the

second subparticle membrane are ruptured, whereby the **reactive** resin and the catalyst **react** to form a conductive adhesive between the first electrical contact and the second electrical contact provided that the coating of the particles interposed between the first **substrate** surface and the second **substrate** surface, but not interposed between the first electrical contact and the second electrical contact, is not broken. This embodiment includes semiconductor dies or chips and semiconductor packages comprising such an interconnect.

Summary of Invention Paragraph - BSTX (17):

[0015] In another preferred embodiment, the invention is an electrical **interconnect comprising: (a) a first substrate having a surface** and at least one first electrical contact projecting from the first **substrate** surface; (b) a second **substrate** having a surface and at least one second electrical contact projecting from the second **substrate** surface and aligned with the first electrical contact, such that the first **substrate** surface is substantially parallel to the second **substrate** surface; and, (c) an adhesive interposed between and in contact with the first electrical contact and the second electrical contact, the adhesive comprising: (1) an electrically non-conductive resin; (2) multiple first particles, each first particle comprising a core comprising at least one **reactive** resin, having an electrically conductive material therein, and a breakable coating of at least one electrically non-conductive material; and (3) multiple second particles, each second particle comprising a core comprising a catalyst and a breakable coating of at least one electrically non-conductive material, wherein the first electrical contact is positioned close enough to the second electrical contact to break the breakable coatings of the first particles and the second

particles in the
interposed adhesive, whereby the reactive resin and the catalyst **react** to form
a conductive adhesive between the first electrical contact and the second
electrical contact, contact provided that the coating of the particles
interposed between the first substrate surface and the second **substrate**
surface, but not interposed between the first electrical contact and the second
electrical contact, is not broken. This embodiment includes semiconductor dies
or chips and semiconductor packages comprising such an interconnect.

Claims Text - CLTX (40):
39. An electrical **interconnect comprising: (a) a first substrate having a**
surface and at least one first electrical contact projecting from the first
substrate surface; (b) a second **substrate** having a surface and at least one
second electrical contact projecting from the second **substrate** surface and
aligned with the first electrical contact, such that the first **substrate**
surface is substantially parallel to the second **substrate** surface; and, (c) a
first adhesive interposed between and in contact with the first electrical
contact and the second electrical contact, the first adhesive comprising an
electrically nonconductive resin and particles, the particles comprising a core
and a breakable coating of at least one electrically non-conductive material,
the core comprising: (1) at least one first subparticle comprising a **reactive**
resin, having conductive material therein, encapsulated inside a rupturable
membrane; and, (2) at least one second subparticle comprising a catalyst
encapsulated inside a rupturable membrane, wherein the first electrical contact
is positioned close enough to the second electrical contact to break the
breakable coating of the particles in the interposed first adhesive such that
the first subparticle membrane and the second subparticle membrane are

ruptured, whereby the **reactive** resin and the catalyst **react** to form a conductive second adhesive between the first electrical contact and the second electrical contact provided that the coating of the particles interposed between the first **substrate** surface and the second **substrate** surface, but not interposed between the first electrical contact and the second electrical contact, is not broken.

Claims Text - CLTX (46):

45. A semiconductor die or chip comprising an electrical interconnect, wherein the electrical **interconnect comprises: (a) a first substrate having a surface** and at least one first electrical contact projecting from the first **substrate** surface; (b) a second **substrate** having a surface and at least one second electrical contact projecting from the second **substrate** surface and aligned with the first electrical contact, such that the first **substrate** surface is substantially parallel to the second **substrate** surface; and, (c) a first adhesive interposed between and in contact with the first electrical contact and the second electrical contact, the first adhesive comprising an electrically nonconductive resin and particles, the particles comprising a core and a breakable coating of at least one electrically non-conductive material, the core comprising: (1) at least one first subparticle comprising a **reactive** resin, having conductive material therein, encapsulated inside a rupturable membrane; and, (2) at least one second subparticle comprising a catalyst encapsulated inside a rupturable membrane, wherein the first electrical contact is positioned close enough to the second electrical contact to break the breakable coating of the particles in the interposed first adhesive such that the first subparticle membrane and the second subparticle membrane are ruptured, whereby the **reactive** resin and the catalyst **react** to form a conductive second adhesive between the first electrical contact and

the second
electrical contact provided that the coating of the particles interposed
between the first **substrate** surface and the second **substrate** surface, but not
interposed between the first electrical contact and the second electrical
contact, is not broken.

Claims Text - CLTX (52):
51. A semiconductor package comprising an electrical interconnect, wherein
the electrical **interconnect comprises: (a) a first substrate having a surface**
and at least one first electrical contact projecting from the first **substrate**
surface; (b) a second **substrate** having a surface and at least one second
electrical contact projecting from the second **substrate** surface and aligned
with the first electrical contact, such that the first **substrate** surface is
substantially parallel to the second **substrate** surface; and, (c) a first
adhesive interposed between and in contact with the first electrical contact
and the second electrical contact, the first adhesive comprising an
electrically nonconductive resin and particles, the particles comprising a core
and a breakable coating of at least one electrically non-conductive material,
the core comprising: (1) at least one first subparticle comprising a **reactive**
resin, having conductive material therein, encapsulated inside a rupturable
membrane; and, (2) at least one second subparticle comprising a catalyst
encapsulated inside a rupturable membrane, wherein the first electrical contact
is positioned close enough to the second electrical contact to break the
breakable coating of the particles in the interposed first adhesive such that
the first subparticle membrane and the second subparticle membrane are
ruptured, whereby the **reactive** resin and the catalyst **react** to form a
conductive second adhesive between the first electrical contact and the second
electrical contact provided that the coating of the particles interposed

between the first **substrate** surface and the second **substrate** surface, but not interposed between the first electrical contact and the second electrical contact, is not broken.

Claims Text - CLTX (64):

63. An electrical **interconnect comprising: (a) a first substrate having a surface** and at least one first electrical contact projecting from the first **substrate** surface; (b) a second **substrate** having a surface and at least one second electrical contact projecting from the second **substrate** surface and aligned with the first electrical contact, such that the first **substrate** surface is substantially parallel to the second **substrate** surface; and, (c) a first adhesive interposed between and in contact with the first electrical contact and the second electrical contact, the second adhesive comprising: (1) an electrically nonconductive resin; (2) multiple first particles, each first particle comprising a core comprising at least one **reactive** resin, having an electrically conductive material therein, and a breakable coating of at least one electrically non-conductive material; and (3) multiple second particles, each second particle comprising a core comprising a catalyst and a breakable coating of at least one electrically non-conductive material, wherein the first electrical contact is positioned close enough to the second electrical contact to break the breakable coatings of the first particles and the second particles in the interposed first adhesive, whereby the **reactive** resin and the catalyst **react** to form a conductive second adhesive between the first electrical contact and the second electrical contact, contact provided that the coating of the particles interposed between the first **substrate** surface and the second **substrate** surface, but not interposed between the first electrical contact and the second electrical contact, is not broken.

Claims Text - CLTX (70):

69. A semiconductor die or chip comprising an electrical interconnect, wherein the electrical **interconnect comprises: (a) a first substrate having a surface** and at least one first electrical contact projecting from the first **substrate** surface; (b) a second **substrate** having a surface and at least one second electrical contact projecting from the second **substrate** surface and aligned with the first electrical contact, such that the first **substrate** surface is substantially parallel to the second **substrate** surface; and, (c) a first adhesive interposed between and in contact with the first electrical contact and the second electrical contact, the second adhesive comprising: (1) an electrically nonconductive resin; (2) multiple first particles, each first particle comprising a core comprising at least one **reactive** resin, having an electrically conductive material therein, and a breakable coating of at least one electrically non-conductive material; and (3) multiple second particles, each second particle comprising a core comprising a catalyst and a breakable coating of at least one electrically non-conductive material, wherein the first electrical contact is positioned close enough to the second electrical contact to break the breakable coatings of the first particles and the second particles in the interposed first adhesive, whereby the **reactive** resin and the catalyst **react** to form a conductive second adhesive between the first electrical contact and the second electrical contact, contact provided that the coating of the particles interposed between the first **substrate** surface and the second **substrate** surface, but not interposed between the first electrical contact and the second electrical contact, is not broken.

Claims Text - CLTX (76):

75. A semiconductor package comprising an electrical

interconnect, wherein
the electrical **interconnect comprises: (a) a first substrate having a surface**
and at least one first electrical contact projecting from the first **substrate**
surface; (b) a second **substrate** having a surface and at least one second
electrical contact projecting from the second **substrate** surface and aligned
with the first electrical contact, such that the first **substrate** surface is
substantially parallel to the second **substrate** surface; and, (c) a first
adhesive interposed between and in contact with the first electrical contact
and the second electrical contact, the first adhesive comprising: (1) an
electrically nonconductive resin; (2) multiple first particles, each first
particle comprising a core comprising at least one **reactive** resin, having an
electrically conductive material therein, and a breakable coating of at least
one electrically non-conductive material; and (3) multiple second particles,
each second particle comprising a core comprising a catalyst and a breakable
coating of at least one electrically non-conductive material, wherein the first
electrical contact is positioned close enough to the second electrical contact
to break the breakable coatings of the first particles and the second particles
in the interposed first adhesive, whereby the **reactive** resin and the catalyst
react to form a conductive second adhesive between the first electrical contact
and the second electrical contact, contact provided that the coating of the
particles interposed between the first **substrate** surface and the second
substrate surface, but not interposed between the first electrical contact and
the second electrical contact, is not broken.